Elektrotechnik

Protection Schemes for Modular Multilevel Converter Based High Voltage Direct Current Transmission System Converters

Xu Jiang

Protection Schemes
for
Modular Multilevel Converter Based
High Voltage Direct Current Transmission System Converters

Von der Fakultät für Ingenieurwissenschaften
der Universität Bayreuth
zur Erlangung der Würde eines
Doktor-Ingenieurs (Dr.-Ing.)
genehmigte Dissertation

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Tag der mündlichen Prüfung: 28.11.2018

Lehrstuhl für Mechatronik
Universität Bayreuth
2018

Berichte aus der Elektrotechnik

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Shaker Verlag
Aachen 2019

Bibliographic information published by the Deutsche Nationalbibliothek
The Deutsche Nationalbibliothek lists this publication in the Deutsche Nationalbibliografie; detailed bibliographic data are available in the Internet at http://dnb.d-nb.de.

Zugl.: Bayreuth, Univ., Diss., 2018

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Printed in Germany.

ISBN 978-3-8440-6450-6
ISSN 0945-0718

Shaker Verlag GmbH • P.O. BOX 101818 • D-52018 Aachen
Phone: 0049/2407/9596-0 • Telefax: 0049/2407/9596-9
Internet: www.shaker.de • e-mail: info@shaker.de

Kurzfassung

Im Vergleich zur Wechselspannung-Übertragung (AC) hat die Hochspannungs-Gleichstrom-Übertragung (HGÜ) sowie Gleichstromverteilung (DC) eine Vielzahl von Vorteilen. Wie z. B. geringe Übertragungsverluste und nicht existente Frequenzunterschiede. In den letzten Jahren haben sich die Hochspannungs-Zwischenkreisumrichter (HV-VSC), HVDC-Technologie und DC-Netze rapide entwickelt. Die Forschung an Multi-Terminal HVDC sowie DC-Netzen, welche auch Gleichstrom-Schalter beinhalten, hat an Wichtigkeit zugenommen. Die Entwicklung von Hochspannungs-Gleichstrom-Schaltern muss dabei eine Vielzahl von Herausforderungen lösen. Diese sind das Nichtvorhandensein eines Stromnulldurchganges, die Herausforderung einen Lichtbogen zu löschen und die geringere Impedanz des DC-Systems im Vergleich zum AC-System. Diese führt im Fehlerfall zu einem schnellen Ansteigen eines Fehlerstromes und weiterhin besteht die Schwierigkeit einer Fehlerdiagnose und Fehlerklärung.

In dieser Dissertation wird eine Übersicht über verschiedene HVDC-Schalter gegeben. Basierend auf dem zugrundenliegenden Prinzip können diese in drei Hauptkategorien eingeteilt werden: Halbleiter basierte Trenner, resonante HVDC-Trenner und hybride HVDC-Trenner. Dabei wird die jeweilige Topologie, ihre Funktionsweise, sowie Vor- und Nachteile diskutiert. Betrachtet wird dabei im Besonderen die Verwendung von HVDC-Trennern in Multi-Terminal-Systemen.

Eine weitere Betrachtung ist die Fehlerklärung mittels eines MMC-Umrichters. Im Vergleich zu 2- und 3-Level Umrichtern ist der MMC vielversprechender. MMC-Umrichter mit Halbbrückensubmodulen haben jedoch keine Fehlerklärungsfähigkeit. Um dieses Problem zu lösen, werden eine Vielzahl von MMC-Topologien vorgeschlagen. Ihre Betriebsweise wird dabei im Detail beschrieben. Der Hybride MMC-Umrichter ist eine Möglichkeit einen Fehler zu blockieren. Weiterhin werden Optimierungen und Modulationsarten vorgestellt. Um die IGBT Abschaltüberspannung in FBSM (Vollbrückensubmodul) zu reduzieren, wird die Methode des „zufälligen“ ersten Blockierens beider Phasen vorgestellt. Durch diese Methode gibt es viele mögliche Ausgangsspannungen eines Arms nach dem ersten Blockieren. Diese führen wiederum zu einer Vielzahl möglicher Steilheiten eines Fehlerstromes. Aus diesem Grund muss ein Schwellwert des maximalen Stromes im Betrieb definiert werden. Hier wird eine Optimierungsmethode der Schwellstrombestimmung vorgeschlagen. Das Verhalten des Fehlerstromes kann dabei anhand der Methode des ersten Blockierens abgeschätzt werden.

Ein neues HVDC Schutzkonzept, welches die Betriebsweise eines HVDC-Trenners und eines MMC-Umrichters kombiniert, wird in dieser Dissertation vorgestellt. In der ursprünglichen Topologie eines MMC-Submoduls wurden Thyristoren zum Überbrücken des Submoduls im Fehlerfall eingesetzt. Dabei wird die verbleibende Fehlerenergie in einem Freilaufkreis abgebaut. In Extremfällen kann der AC-Trenner bei einem Kurzschluss auf AC-Seite geöffnet werden. Eine Ein-Ableiter Version des vorgeschlagenen Schutzkonzeptes klärt den DC-Fehlerfall in kürzester Zeit. Gleichzeitig wird der DC-Fehlerstrom in den Freilaufdioden reduziert. Dieses Konzept hat jedoch auch Nachteile, welche den Schwarzstart eines HVDC-Systems betreffen. Aus diesem Grund wird die Zwei-Ableiter Version vorgeschlagen, welche den DC-Kurzschluss klärt und dabei in kurzer Zeit ebenso die Fehlerenergie der DC-Seite aufnimmt. Durch die Berechnung der Verlustleistung der verschiedenen Schutzkonzepte wird deutlich, dass das neue Schutzkonzept eine geringere Verlustleistung aufweist bei gleichzeitiger Verbesserung des Betriebsverhaltens.

Abstract

Compared with alternating current (AC) power transmission and distribution, high-voltage direct current transmission (HVDC) and the direct current (DC) distribution have a series of advantages, such as low line loss and the absence of the synchronous operation problem. In recent years, as with the rapid development of the high-voltage voltage-source converter (HV-VSC), HVDC technology, and DC distribution, the study of flexible multi-terminal HVDC and DC distribution technologies as well as high-voltage DC circuit breakers has been highly prized. The development of high-voltage DC circuit breakers must solve many major problems: there is no zero-crossing in DC current, and the DC arc is difficult to extinguish; the impedance of a DC system (in steady state founded by resistance only) is much smaller than an AC system, which results in a fast-growing short-circuit (especially in the DC system based on VSC) and furthermore compounds the difficulty of fault diagnosis and short-circuit current interruption.

This dissertation introduces a technical overview of the HVDC breaker. Based on the working principle, there are mainly three kinds of HVDC breakers: the all-solid HVDC breaker, the resonance HVDC breaker and the hybrid HVDC breaker. Their topologies, working principle, advantages and disadvantages are presented. A comparison of different HVDC breakers based on their functions is also made, which includes the usage of HVDC breakers in multi-terminal HVDC systems.

Another direction of dealing with DC faults is based on MMC converters. Compared with two-level and three-level converters, the MMC is more promising. However, HB-MMC doesn't have fault ride-through capability. In order to solve this problem, many kinds of MMC topologies are proposed, and their working principles are illustrated with more details. Hybrid MMC is also an important method to block the fault current. The optimization and modulation method are also introduced. In order to reduce the over-voltage of IGBTs in FBSMs (and also other modified topologies), the random first blocking of both sides in FBSMs is proposed. Because of this method, there are many possible output voltages in each arm after the first blocking, which also leads to many possible fault-current slopes. For this reason, the threshold current should be determined to avoid exceeding the maximum turn-off current. In order to increase the anti-disturbance ability, an optimization method of threshold current is proposed. The fault-current behaviour can be attained according to this first blocking method.

A new HVDC protection scheme is presented in this dissertation; it combines the principle of HVDC breaker and MMC topology. The original topology uses a double-thyristor-switch MMC sub-module to cut off the energy flow from the AC side to the DC side. The rest energy is consumed in the fault-current loop. However, for some extreme cases, the AC breaker could be opened because of a long-time short-circuit in the AC side. Hence, a one-arrestor version of the new protection scheme is developed to cut off the DC short circuit in a short time, and the DC fault current is reduced in a free-wheeling diodes loop. This scheme also has a disadvantage, which could affect the restart of the HVDC system in extreme cases. For this reason, the two-arrestor version is proposed, which can cut off the DC short circuit and consume rest energy in the DC line in a short time. According to the calculation, the loss power for different protection schemes can be attained and compared. The new protection scheme has less loss power than most schemes, and it also overcomes disadvantages of others.

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Acronyms

AC	alternating current
CB	circuit breaker
CDSM	clamp-double sub-module
CSC	current source converter
DC	direct current
FB	full-bridge
FLCC	five level cross connected cell type
FLCT	four level MMC cell type
GTO	gate turn-off thyristor
HB	half-bridge
HVDC	high-voltage direct current
IGBT	insulated-gate bipolar transistor
IGCT	integrated gate-commutates thyristor
KVL	Kirchhoff's voltage law
LCC	Line-commutated converter
LCS	load commutation switch
MMC	modular multilevel converter
MOV	Metal Oxide Varistor
MOS	metal-oxide semiconductor
NPC	neutral point clamped
PLUS	power link universal system
PWM	pulse-width modulation
SM	sub-module
THD	total harmonic distortion
UFD	ultra-fast disconnector
VSC	voltage source converter

Symbols

C	
C	Capacitance
C_1	Capacitance of first capacitor in two capacitor cell
C_2	Capacitance of second capacitor in two capacitor cell
$\cos\varphi$	Power factor
C_{HW}	Total hardware cost
C_{tot}	Total cost per 1 MW
E	
$E_{HB,s1}$	Energy is converted by the HBSMs
E_{On}	Turn-on loss energy of IGBT
E_{Off}	Turn-off loss energy of IGBT
E_{RR}	Reverse-recovery loss energy of diode
F	
FVD	Forward voltage drop of diode
F_{FB}	Hardware cost factor of FB
F_{HB}	Hardware cost factor of HB
F_{med}	Medium cost factor rating
f_S	Switching frequency
f_N	AC grid frequency
I	
i_z $(z = a, b, c)$	Phase current in phase a, b and c
I_A	Current of anode
i_B	Current in breaker
I_C	Current of collector
i_{CE}	Collector-emitter current
i_D	Instantaneous diode current
I_{DC}	Rate DC current of HVDC system
I_H	Holding current
I_F	Forward current
I_{RRM}	Peak reverse recovery current
$i_{arm,k}$	Current in arm_k of MMC, k=1,2,3,4,5,6
i_{SM}	Current through the sub-module in MMC
i_{AC}	AC side current
$\hat{I}_{AC}$	Peak value of AC side current
$i_{Arm,p}$	Current of upper arm
$i_{Arm,n}$	Current of lower arm
I_0	Initial current
i_{res}	Resonant current
i_{MOV}	Current through MOV
$I_{DC,max}$	Current rating, which leads to a junction temperature T_J=125°C of a semiconductor
i_T	Initial current of SM before the first blocking
$I_{arm1,max}$	Maximum possible fault current in arm_1
I_{max}	Maximum possible fault current in certain arm
I_t	Threshold current
I_{pt}	Pre-threshold current
i_{SC}	Short circuit current
$I_{DC,\mathrm{I}}$	DC current in branch Ⅰ

$I_{DC,II}$	DC current in branch II
I_D	Current through free-wheeling diodes
K	
K_S	Safety factor
L	
L	Inductance
L_{arm}	Inductance in each arm of MMC
L_{AC}	Inductance of AC side in each phase
L_{DC}	Total inductance in DC line
L_{HB}	Operating losses of HB
L_{FB}	Operating losses of FB
M	
m	Modulation index
N	
n_0	Minimum needed amount of cells in one single arm
n	Number of sub-modules in each arm in MMC
N_b	Number of minimum needed FBSMs
n_{HB}	Number of half-bridge sub-modules in each arm
N_{HB}	Optimum number of HBSMs in each arm
n_{FB}	Number of full-bridge sub-modules in each arm
N_{FB}	Optimum number of FBSMs in each arm
N_{tot}	Number of SMs in each arm after the optimization
n_N	Number of full-bridge sub-modules are allowed to generate negative voltage in each arm
P	
P_{AC}	AC power
P_C	Conduction loss of HVDC breaker
P_{DC}	Transmitted DC power
p_{CE}	Instantaneous conduction loss of IGBT
p_D	Instantaneous conduction loss of diode
$P(U_{arm_{k,1}})$	Probability for the arm voltage after the first blocking in arm_k
P_{slope}	Probability for certain slope after the first blocking
P_L	Total loss energy of MMC based protection schemes
$P_{C,T_x/D_x}$	Conduction losses of each IGBT and diode
R	
R_{CE}	Collector-emitter on-state resistance
R_{on}	Diode on-resistance
R_{arm}	Resistance in each arm
S	
S	Apparent power
T	
t_{ac}	AC short circuit duration
$t_{dcdecay}$	DC current decay time
$t_{dc1decay}$	DC current decay time in UFD
t_{UFDoff}	Turn-off time of UFD

t_{acoff}	Duration of turning off AC overcurrent
$t_{d(on)}$	Turn-on decay time
t_{fr}	Forward recovery time
t_{fi1}	Time interval of rapid drop in the IGBT current
t_{fi2}	Tailing of the collector current
t_{fv1}	1st interval of decreasing time of collector-to-emitter voltage
t_{fv2}	2nd interval of decreasing time of collector-to-emitter voltage
t_{rr}	Reverse recovery time
t_{gt}	Gate-controlled turn-on time
t_{gd}	Gate-controlled delay time
t_{gr}	Gate-controlled rise time
t_q	Circuit-commutates turn-off time
t_{ri}	Current rise time
T_{open}	The time of turn off the fault current
T_J	Junction temperature
U	
u_{AC}	Voltage of AC side
$\hat{U}_{AC}$	Peak value of AC side voltage
U_C	Voltage of capacitor in the sub-module
U_{cell}	Voltage of cell voltage of MMC
U_{DC}	Rate DC voltage of HVDC system
$u_{arm,k}$	Voltage in arm_k of MMC, k=1,2,3,4,5,6
$u_{Arm,p}$	Voltage of upper arm
$u_{Arm,n}$	Voltage of lower arm
U_L	Voltage of inductor
u_{max}	Peak line-to-line AC voltage for the MMC during a DC fault at maximum modulation index
U_{FB}	Voltage of FBSMs in each arm of hybrid MMC
U_{HB}	Voltage of HBSMs in each arm of hybrid MMC
U_T	Initial voltage of SM before the first blocking
$U_{T,1}$	Voltage of SM after the first blocking
$U_{T,2}$	Voltage of SM after the second blocking
$U_{arm_{k,1}}$	Arm voltage in arm_k after the first blocking
u_{0i}	Output voltage of the new sub-modules during the fault
u_{ab}	Line-to-line grid voltage between phase A and phase B
U_{ll}	peak value of the line-to-line grid
u_z $(z = a, b, c)$	Phase voltage of phase a, b and c
$u_{arrestor}$	Clamped voltage of arrestor
V	
V_B	Blocking voltage of FBSMs after the fault
V_b	Arc voltage between the breaker
V_{CE}	Collector-emitter voltage
V_{DC}	DC voltage source
V_{c1}	Voltage of first capacitor in two capacitors cell
V_{c2}	Voltage of second capacitor in two capacitors cell
V_F	Forward voltage

V_{FRM}	Maximum turn-on voltage
V_R	Reverse voltage
V_{GE}	Gate-emitter voltage
v_D	Voltage drop over the diode
W	
W_R	Absorbed energy in arrestors
X	
X_k	Number of inserted FBSMs in arm_k of hybrid MMC before the first blocking
Y	
Y_k	Number of bypassed FBSMs in arm_k of hybrid MMC before the first blocking
Z	
Z_k	Number of HBSM in arm_k of hybrid MMC before the first blocking
Greek alphabet	
α_i	Firing angle of thyristors
ω	Angular frequency
φ_k	Phase angles in arm_k, k=1,2,3,4,5,6
φ_i	Angle between voltage and current in each arm
φ_N	AC grid power angle
τ	Time constant
δ_{cell}	Average duty-cycle of a cell
δ_k	Duty cycle of state k
δ_{HB}	Duty cycle of HBSMs