Analog Circuit Design in PD-SOI CMOS Technology for High Temperatures up to 400 °C using Reverse Body Biasing (RBB)

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Abstract

This work focuses on analog integrated CMOS (Complementary Metal-Oxide-Semiconductor) circuit design in SOI (Silicon on Insulator) technology for the use in high temperature applications. It investigates the influence of reverse body biasing (RBB) on the analog characteristics of SOI-MOSFET (Metal-Oxide-Semiconductor-Field-Effect-Transistor) transistors. Additionally, the enhancement of the operation capability of fundamental analog circuits at high temperatures up to 400 °C with the use of RBB is investigated.

Analog and digital integrated circuits are used in a variety of applications, e.g. consumer electronics or industrial measurement equipment. These integrated circuits have to work properly in the temperature range predefined by the application. As an example, operating temperatures reaching from −50 °C to 250 °C are required for geothermal drilling applications. Currently in the automotive industry, electronics have to operate reliably up to 150 °C and as control electronics are placed closer to the engine, a much higher operating temperature is required. High temperature electronics are also used in avionic- and space applications, e.g. for future venus exploration missions, where they have to withstand operating temperatures of 300 °C to 500 °C. Active or passive cooling of electronic components requires additional space and weight that increases the cost of the overall system. Cooling can be avoided in case electronics are capable of operating in harsh environmental conditions, i.e. at high temperatures.

SOI-MOSFET devices are theoretically capable of operation up to 400 °C or even higher, depending on the doping concentration of the silicon film. Nearly all material and device properties of importance to electronics worsen with increasing temperature, which is why 300 °C to 350 °C is the currently stated experimental maximum operating temperature of SOI devices. Analog circuit design up to the theoretical temperature limit exhibits severe limitations as SOI-MOSFET device characteristics are degenerated. SOI-MOSFET devices are partially depleted (PD) or fully depleted (FD), depending on the temperature, doping concentration of the silicon film, silicon film thickness and also channel length. FD devices offer a much

better analog performance compared to their partially depleted counterparts and are preferred for analog circuit design. In the considered SOI technology, SOI-MOSFET devices are FD at low temperatures and PD at high temperatures. The transition from FD to PD at high temperatures leads to increased device leakage currents and hence reduces the overall performance of the transistor devices. Thereby, the g_m/I_d factor as a major figure of merit is decreased dramatically at high temperatures. Especially the moderate inversion region, which offers high intrinsic gain and moderate intrinsic bandwidth, is strongly affected as device leakage currents exceed the range of device operating currents at high temperatures.

Reverse body biasing (RBB) refers to the reverse biasing of the film-source PN-junction of a MOSFET transistor. In recent works, reverse body biasing has been applied to digital circuits in order to reduce the static current consumption. Reverse body biasing has also been investigated in the analog domain. Nevertheless, the importance of the technique to realize analog circuits capable of operating at the theoretical temperature limit of SOI technology has not been identified yet. SOI-MOSFET devices with an H-shaped gate are investigated in a 1.0 µm PD-SOI technology. These devices provide a body-contact, which is used to apply the reverse body bias. It is found that due to the use of RBB, these devices remain fully depleted in the considered temperature range up to 400 °C. Due to the reduction of leakage currents, reverse biased SOI-MOSFET devices are capable of operating in the mid moderate inversion region, with an operating current of one fifth of the leakage current level which was measured without RBB. This results in an improved g_m/I_d factor and an increase of the intrinsic gain by approximately 14 dB. Besides the investigation of SOI-MOSFET device characteristics, reverse body biasing is also applied to fundamental analog building blocks, e.g. an analog switch, current mirrors, a two-stage operational amplifier and a first order bandgap voltage reference. It is found that reverse body biasing significantly improves the high temperature operation of these circuits. In summary, the proposed technique of reverse body biasing offers the possibility to achieve FD device characteristics in a PD-SOI technology and thereby to improve the performance of analog circuits at high temperatures up to 400 °C.

Contents

Abbrevations

ABB	Adaptive body biasing
AC	Alternating current
ADC	Analog-to-digital converter
B	Body terminal
BEX	Mobility temperature exponent
BG	Back gate terminal
BJT	Bipolar junction transistor
BNC	Bayonet Neill Concelman connector
BPSG	Borophosphosilicate glass
BSIMSOI	BSIMSOI is a SPICE compact model for SOI circuit design
BT PD-SOI ...	Body tied partially depleted silicon on insulator
CLM	Channel length modulation
CM	Current mirror
CMOS	Complementary metal-oxide-semiconductor
D	Drain terminal
DC	Direct current
DD	Dynamically depleted
DIBL	Drain-induced barrier lowering

EEPROM ..... Electronically erasable and programmable read only memory

FBB ..... Forward body biasing

FD ..... Fully depleted

FinFET ..... Fin field-effect-transistor

FOX ..... Field-oxide

G ..... Gate terminal

GOX ..... Gate oxide

GPIB ..... General purpose interface bus / IEEE-488

HGATE ..... H-shaped gate SOI-MOSFET

HT ..... High temperature

IC ..... Inversion coefficient

`Isbjt` ..... BSIMSOI model parameter for BJT injection saturation current

`Isrec` ..... BSIMSOI model parameter for recombination in depletion saturation

`K1` ..... BSIMSOI model parameter for first order body effect coefficient

LOCOS ..... Local oxidation of silicon

MI ..... Moderate inversion

MOSFET ..... Metal-oxide-semiconductor-field-effect-transistor

`Nch` ..... BSIMSOI model parameter for the doping concentration of the silicon film

`Nfactor` ..... BSIMSOI model parameter for the subthreshold swing factor

NHGATE ..... N-channel HGATE SOI-MOSFET

NSOI	N-channel Split-Source SOI-MOSFET
op-amp	Operational amplifier
PCB	Printed circuit board
PD	Partially depleted
PHGATE	P-channel HGATE SOI-MOSFET
PID-Controller	Proportional-integral-derivative controller
PSOI	P-channel Split-Source SOI-MOSFET
PTAT	Proportional to absolute temperate
PoR	Power-on reset
RBB	Reverse body biasing
RF	Radio frequency
RFID	Radio frequency identification
RPOLY	Poly-silicon resistor
RPPLUS	P^+ implanted resistor
S	Source terminal
SCE	Short-channel-effects
SI	Strong inversion
SIMOX	Separation by implantation of oxygen
SOI	Silicon on insulator
`soimod`	BSIMSOI model selector
SSCB	Silicon sidewall body contact
`Tbox`	BSIMSOI model parameter for the buried oxide thickness
`Tox`	BSIMSOI model parameter for the gate oxide thickness

`Tsi` ..... BSIMSOI model parameter for the silicon film thickness

UTB ..... Ultra thin body

VLSI ..... Very large scale integration

WI ..... Weak inversion

ZTC ..... Zero temperature coefficient

List of Symbols

β ..... Bipolar current gain

χ_{SI} ..... Electron affinity of silicon

$\Delta\phi$ ..... Portion of surface potential to reach strong inversion

ΔV_{bi} ..... Built-in potential lowering in FD SOI-MOSFETs

ϵ_0 ..... Dielectric constant in vacuum $8.85 \cdot 10^{-9}\,\frac{\mathrm{F}}{\mathrm{m}}$

ϵ_{ox} ..... Dielectric constant of silicon-oxide $3.9 \cdot \epsilon_0$

ϵ_{si} ..... Dielectric constant of silicon $11.9 \cdot \epsilon_0$

γ ..... Body effect coefficient

$\hat{C}_{GBi}$ ..... Intrinsic gate-body capacitance normalized to the gate-oxide capacitance

$\hat{C}_{GSi}$ ..... Intrinsic gate-source capacitance normalized to the gate-oxide capacitance

λ ..... Channel length modulation factor

μ_0 ..... Zero-field mobility of charge carriers

μ_{T0} ..... Zero-field mobility of charge carriers at 300K

$\phi(x)$ ..... Surface potential as a function of silicon film depth

ϕ_F ..... Fermi potential

ϕ_S ..... Surface potential

ϕ_{bi} ..... Built-in potential of a pn-junction

ϕ_{Fn} ..... Fermi potential of a n-type semiconductor

ϕ_{Fp} ..... Fermi potential of a p-type semiconductor

ϕ_{ms1} ..... Front gate metal semiconductor work function difference

ϕ_{ms2} ..... Back gate metal semiconductor work function difference

ϕ_{ms} ..... Metal semiconductor work function difference

ϕ_{S1} ..... Front gate surface potential

ϕ_{S2} ..... Back gate surface potential

τ_g ..... Lifetime of generated charges in the depletion region

τ_n ..... Lifetime of electrons

τ_p ..... Lifetime of holes

A_i ..... Intrinsic gain

C'_D ..... Depletion capacitance per unit area

C'_{OX1} ..... Front gate oxide capacitance per unit area

C'_{OX2} ..... Back gate oxide capacitance per unit area

C_{DBi} ..... Intrinsic drain-body capacitance

C_{DSi} ..... Intrinsic drain-source capacitance

C_{GBi} ..... Intrinsic gate-body capacitance

C_{GDi} ..... Intrinsic gate-drain capacitance

C_{GSi} ..... Intrinsic gate-source capacitance

C_L ..... Load capacitance

C_{OX1} ..... Front gate oxide capacitance

C_{OX2} ..... Back gate oxide capacitance

C_{SBi} ..... Intrinsic source-body capacitance

C_{si} ..... Capacitance of the fully depleted silicon film

D_n ..... Diffusion constant of electrons

E ..... Energy level

E_C ..... Conduction band energy

$E_G(0)$ ..... Bandgap energy at absolute zero temperature (0 K)

E_V ..... Valence band energy

E_F ..... Fermi energy

E_G ..... Bandgap energy

E_i ..... Intrinsic Fermi energy level

F_E ..... Fermi-Dirac distribution function

f_T ..... Intrinsic bandwidth / Transition frequency

g_m/I_d ..... Transconductance efficiency

g_{ds} ..... Drain-source small signal conductance

g_{mb} ..... Body-source small signal transconductance

g_{mMAX} ..... Maximum small signal transconductance

g_m ..... Small signal transconductance

I_0 ..... Technology current

I_0 (fit) ..... Technology current used for fitting

i_f ..... Specific current, equivalent to I_0

I_{Bbjt} ..... Base current of parasitic bipolar transistor

I_B ..... Body current

I_{CH} ..... Current in the inverted channel

I_C ..... Collector current

I_{DIFF} ..... Diffusion current

I_{dsat} ..... Saturation current

I_d ..... Drain current

I_E ..... Emitter current

I_{Gmax} ..... Generation current at maximum depletion depth

I_G ..... Generation current

I_{ii} ..... Impact ionization current

I_{IN} ..... Input current

I_L ..... Leakage current

I_{OFF} ..... MOSFET off-state current

I_{ON} ..... MOSFET on-state current

I_{OUT} ..... Output current

I_{PN-N} ..... PN-junction leakage current of N-channel device

I_{PN-P} ..... PN-junction leakage current of P-channel device

I_{PN} ..... PN-junction leakage current

I_{PTAT} ..... Proportional to absolute temperature current

I_{Sub-N} ..... Subthreshold leakage current of N-channel device

I_{Sub-P} ..... Subthreshold leakage current of P-channel device

I_{Sub} ..... Subthreshold leakage current

I_S ..... Source current

k ..... Boltzmann constant $8.617 \cdot 10^{-5}\,\frac{\mathrm{eV}}{\mathrm{K}}$

L ..... Channel length

L_B ..... Base region length

L_n ..... Diffusion length of electrons

n ..... Body factor

$n\,(\mathrm{fit})$ ..... Body factor used for fitting

N_A ..... Doping concentration of p-type silicon

N_{CH} ..... Channel doping concentration

N_{DRAIN} ..... Doping concentration of drain region

N_D ..... Doping concentration of n-type silicon

n_{FD} ..... Body factor in fully depleted mode

N_I ..... Intrinsic region in PIN-diodes

n_i ..... Intrinsic carrier concentration

n_{n0} ..... Electron concentration in n-type silicon

n_{p0} ..... Electron concentration in p-type silicon

n_{PD} ..... Body factor in partially depleted mode

N_{SOURCE} ... Doping concentration of source region

N_{Sub} ..... Effective substrate doping concentration

p_{n0} ..... Hole concentration in n-type silicon

p_{p0} ..... Hole concentration in p-type silicon

q ..... Electron charge $1.602 \cdot 10^{-19}\,\mathrm{C}$

Q'_d ..... Depletion charge per unit area

Q_d ..... Depletion charge

Q_{ox1} ..... Front gate oxide charges

Q_{ox2} ..... Back gate oxide charges

R_B ..... Body resistance

r_{ds} ..... Small signal drain-source resistance

R_L ..... Load resistance

R_{out} ..... Output resistance

R_S ..... Source resistance

S ..... Subthreshold swing

S_{FD} ..... Subthreshold swing in fully depleted mode

S_{PD} ..... Subthreshold swing in partially depleted mode

T ..... Temperature

T_0 ..... Reference temperature

T_t ..... Transition temperature

t_{BOX} ..... Back gate oxide (buried oxide) thickness

t_{OX1} ..... Front gate oxide thickness

t_{SI} ..... Silicon film thickness

TK_1 ..... First order (linear) temperature coefficient

TK_2 ..... Second order (quadratic) temperature coefficient

V_A ..... Early voltage

V_b ..... Body potential

V_t ..... Thermal voltage

V_{BGS} ..... Back gate-source voltage

V_{bi} ..... Built-in voltage of a pn-junction

V_{BN} ..... Body bias voltage for N-channel devices

V_{BP} ..... Body bias voltage for P-channel devices

V_{BSminN} .... Required minimum reverse bias voltage for N-channel devices

V_{BSminP} ..... Required minimum reverse bias voltage for P-channel devices

V_{BSmin} ..... Required minimum reverse bias voltage

V_{BSN} ..... Body-source voltage for N-channel devices

V_{BSP} ..... Body-source voltage for P-channel devices

V_{BS} ..... External body-source voltage

v_{bs} ..... Small signal body-source voltage

V_{CM} ..... Common mode voltage

V_{DDA} ..... Supply voltage of analog circuits

V_{DSsat} ..... Drain-source saturation voltage

V_{DS} ..... Drain-source voltage

v_{ds} ..... Small signal drain-source voltage

V_{FB1} ..... Front gate flatband voltage

V_{FB2} ..... Back gate flatband voltage

V_{FB} ..... Flatband voltage

V_{G1} ..... Front gate voltage

V_{G2acc} ..... Back gate voltage, at which the back interface becomes accumulated

V_{G2} ..... Back gate voltage

V_{GNDA} ..... Ground potential in analog circuits

V_{GS1} ..... Front gate-source voltage

V_{GS} ..... Gate-source voltage

v_{gs} ..... Small signal gate-source voltage

V_{IN} ..... Input voltage

v_{in} ..... Small signal input voltage

V_{OUT} ..... Output voltage

v_{out} ..... Small signal output voltage

V_{REF} ..... Reference output voltage

V_{th1} ..... Front gate threshold voltage

V_{th2} ..... Back gate threshold voltage

W ..... Channel width

W_{eff} ..... Effective channel width

x_{d1max} ..... Front gate depletion depth in strong inversion

x_{d1} ..... Front gate depletion depth

x_{d2} ..... Back gate depletion depth

phi ..... clock signal for analog switch

sgn ..... Signum function

List of Tables

List of Figures