Analog Circuit Design in PD-SOI CMOS Technology for High Temperatures up to 400 °C using Reverse Body Biasing (RBB)

Von der Fakultät für Ingenieurwissenschaften Abteilung Elektrotechnik und Informationstechnik der Universität Duisburg-Essen

zur Erlangung des akademischen Grades

Doktor der Ingenieurwissenschaften

genehmigte Dissertation

von

Alexander Schmidt

aus

Lich

1. Gutachter:Prof. Dr. R. Kokozinski2. Gutachter:Prof. Dr. H. Fiedler

Tag der mündlichen Prüfung: 27.01.2014

Berichte aus der Elektrotechnik

Alexander Schmidt

Analog Circuit Design in PD-SOI CMOS Technology for High Temperatures up to 400°C using Reverse Body Biasing (RBB)

> Shaker Verlag Aachen 2015

Bibliographic information published by the Deutsche Nationalbibliothek

The Deutsche Nationalbibliothek lists this publication in the Deutsche Nationalbibliografie; detailed bibliographic data are available in the Internet at http://dnb.d-nb.de.

Zugl.: Duisburg-Essen, Univ., Diss., 2014

Copyright Shaker Verlag 2015 All rights reserved. No part of this publication may be reproduced, stored in a retrieval system, or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording or otherwise, without the prior permission of the publishers.

Printed in Germany.

ISBN 978-3-8440-3853-8 ISSN 0945-0718

Shaker Verlag GmbH • P.O. BOX 101818 • D-52018 Aachen Phone: 0049/2407/9596-0 • Telefax: 0049/2407/9596-9 Internet: www.shaker.de • e-mail: info@shaker.de

Acknowledgments

This work was created at the department of *Integrated Circuits and Systems (ISS)* of the Fraunhofer Institute for Microelectronic Circuits and Systems (IMS) in Duisburg, Germany. My deepest gratitude goes to my research supervisor, Prof. Dr. Rainer Kokozinski, for his support throughout my time in the ISS department. I would also like to thank Prof. Dr. Anton Grabmaier for the opportunity to work in this interesting research context. My gratitude goes also to Prof. Dr. Horst Fiedler for becoming the second examiner of this work.

In particular, I want to thank Holger Kappert, group leader of the *High-Temperature Electronics* group at Fraunhofer IMS, for his enthusiastic support, invaluable discussions and encouraging comments on my research proposal. He was also a constructive critic in the best sense.

This investigation would have never been completed without the help and important suggestions of the people around me in the entire ISS department. For providing their help and knowledge in various discussions, I would like to thank especially Dr. Norbert Kordas, Abdel Moneim Marzouk, Kishore Meduri Venkata Subramanya, Dr. Stefan Dreiner, Dr. Uwe Paschen, Dr. Katharina Grella, Andre Kosfeld, Reneé Lerch, Dr. Andre Lüdecke, Ralf Thiel, Dirk Dittrich, Jidan Al-Eryani, Christian Al-Haddad, Michael Alfring, Susanne Kittner, Tatjana Fedtschenko, Dr. Miriam Klusmann, Dr. Sascha Weyers and all student assistants. I would like to thank my family for their love and support. Finally, I thank Maria for her lovingly support and patience. This work is dedicated to her.

Abstract

This work focuses on analog integrated CMOS (Complementary Metal-Oxide-Semiconductor) circuit design in SOI (Silicon on Insulator) technology for the use in high temperature applications. It investigates the influence of reverse body biasing (RBB) on the analog characteristics of SOI-MOSFET (Metal-Oxide-Semiconductor-Field-Effect-Transistor) transistors. Additionally, the enhancement of the operation capability of fundamental analog circuits at high temperatures up to 400 °C with the use of RBB is investigated.

Analog and digital integrated circuits are used in a variety of applications, e.g. consumer electronics or industrial measurement equipment. These integrated circuits have to work properly in the temperature range predefined by the application. As an example, operating temperatures reaching from -50 °C to 250 °C are required for geothermal drilling applications. Currently in the automotive industry, electronics have to operate reliably up to 150 °C and as control electronics are placed closer to the engine, a much higher operating temperature is required. High temperature electronics are also used in avionicand space applications, e.g. for future venus exploration missions, where they have to withstand operating temperatures of 300 °C to 500 °C. Active or passive cooling of electronic components requires additional space and weight that increases the cost of the overall system. Cooling can be avoided in case electronics are capable of operating in harsh environmental conditions, i.e. at high temperatures.

SOI-MOSFET devices are theoretically capable of operation up to 400 °C or even higher, depending on the doping concentration of the silicon film. Nearly all material and device properties of importance to electronics worsen with increasing temperature, which is why 300 °C to 350 °C is the currently stated experimental maximum operating temperature of SOI devices. Analog circuit design up to the theoretical temperature limit exhibits severe limitations as SOI-MOSFET device characteristics are degenerated. SOI-MOSFET devices are partially depleted (PD) or fully depleted (FD), depending on the temperature, doping concentration of the silicon film, silicon film thickness and also channel length. FD devices offer a much better analog performance compared to their partially depleted counterparts and are preferred for analog circuit design. In the considered SOI technology, SOI-MOSFET devices are FD at low temperatures and PD at high temperatures. The transition from FD to PD at high temperatures leads to increased device leakage currents and hence reduces the overall performance of the transistor devices. Thereby, the g_m/I_d factor as a major figure of merit is decreased dramatically at high temperatures. Especially the moderate inversion region, which offers high intrinsic gain and moderate intrinsic bandwidth, is strongly affected as device leakage currents exceed the range of device operating currents at high temperatures.

Reverse body biasing (RBB) refers to the reverse biasing of the film-source PN-junction of a MOSFET transistor. In recent works, reverse body biasing has been applied to digital circuits in order to reduce the static current consumption. Reverse body biasing has also been investigated in the analog domain. Nevertheless, the importance of the technique to realize analog circuits capable of operating at the theoretical temperature limit of SOI technology has not been identified yet. SOI-MOSFET devices with an H-shaped gate are investigated in a 1.0 µm PD-SOI technology. These devices provide a body-contact, which is used to apply the reverse body bias. It is found that due to the use of RBB, these devices remain fully depleted in the considered temperature range up to 400 °C. Due to the reduction of leakage currents, reverse biased SOI-MOSFET devices are capable of operating in the mid moderate inversion region, with an operating current of one fifth of the leakage current level which was measured without RBB. This results in an improved g_m/I_d factor and an increase of the intrinsic gain by approximately 14 dB. Besides the investigation of SOI-MOSFET device characteristics, reverse body biasing is also applied to fundamental analog building blocks, e.g. an analog switch, current mirrors, a two-stage operational amplifier and a first order bandgap voltage reference. It is found that reverse body biasing significantly improves the high temperature operation of these circuits. In summary, the proposed technique of reverse body biasing offers the possibility to achieve FD device characteristics in a PD-SOI technology and thereby to improve the performance of analog circuits at high temperatures up to 400 °C.

Contents

A	bbrev	vations	5										xi
\mathbf{Li}	st of	Symb	ols										xv
\mathbf{Li}	st of	Tables	3									x	xiii
\mathbf{Li}	st of	Figure	es									х	xv
1	Intr	oducti	on										1
	1.1	Motiva	ation										1
	1.2	State of	of the Art \ldots \ldots \ldots \ldots \ldots \ldots										4
	1.3	Thesis	Outline	•	•		•	•		•		•	7
2	SOI	СМО	S Technology										8
	2.1	Device	es in SOI CMOS Technology										9
		2.1.1	Split-Source Transistor										10
		2.1.2	HGATE Transistor										12
		2.1.3	PIN-Diode										13
		2.1.4	P^+ Implanted Resistor (RPPLUS)										13
		2.1.5	Poly-Silicon Resistor (RPOLY)										14
		2.1.6	Capacitor	•	•	 •	•	•	•	•	•	•	15
3	Fun	damen	tals of SOI-MOSFETs										16
	3.1	Carrie	r Concentration at Thermal Equilibrium										16
	3.2	Deplet	ion States and Surface Potentials										18
		3.2.1	Partially depleted Devices										20
		3.2.2	Fully depleted Devices										24
	3.3	Body	factor										26
	3.4	Subth	reshold Swing										27
	3.5	PN-Ju	nctions										28
		3.5.1	Built-In Potential										28
		3.5.2	Built-In Potential Lowering										30
		3.5.3	Depletion Width										31
	3.6	Thresh	nold Voltage of SOI-MOSFETs										32
		3.6.1	Partially Depleted										32
		3.6.2	Fully Depleted										33
	3.7	Body-	Effect										35

	3.8	Leakage Currents	36
		3.8.1 PN-Junction Leakage Current	37
		3.8.2 Subthreshold Leakage Current	38
		3.8.3 Sidewall Leakage Current	40
	3.9	Floating Body-Effects	41
		3.9.1 Kink-Effect	42
		3.9.2 Parasitic Bipolar-Effect	43
	3.10	The q_m/I_d Figure of Merit	44
		3.10.1 q_m/I_d Factor in all Regions of Operation	45
		3.10.2 Technology Current	48
		3.10.3 Inversion Coefficient	48
	3.11	Intrinsic Gain and Intrinsic Bandwidth	49
	3.12	Early Voltage	51
	3.13	Summary	52
		v	
4	SOL	-MOSFET Characteristics in a Wide Temperature Range	54
	4.1	Limitations of SOI Technology	54
	4.2	Threshold Voltage at High Temperatures	56
	4.3	Leakage Currents	58
	4.4	SOI-MOSFET Performance	60
		4.4.1 g_m/I_d Factor at High Temperatures	61
		4.4.2 Technology Current at High Temperatures	65
		4.4.3 Early Voltage at High Temperatures	68
		4.4.4 Intrinsic Gain at High Temperatures	71
		4.4.5 Intrinsic Bandwidth at High Temperatures	73
	4.5	I_{ON}/I_{OFF} Ratio	75
	4.6	Summary	77
5	Ana	log Circuits in a Wide Temperature Bange	78
Ő	5.1	Fundamental Analog Building Blocks	80
	0.1	51.1 Analog Switches	80
		51.2 Current Mirrors	83
		51.3 Operational Amplifiers	86
		5.1.4 Voltage References	88
	5.2	Summary	91
6	Imp	roved SOI-MOSFET Characteristics at High Temperatures	93
	6.1	Reverse Body Biasing (RBB)	93
	6.2	Depletion State of the Silicon Film	94
	6.3	Minimum Reverse Bias Voltage	97
	6.4	Surface Potentials	99
	6.5	Body Factor	105
	6.6	Threshold Voltage	106
	6.7	PN-Junction Leakage Current	109
	60	Subthrashold Lashaga Current	111
	0.0	Subtilieshold Leakage Current	111
	0.8 6.9	Output Conductance in Off-State	112

	6.11	I_{ON}/I_{OFF} Ratio	116
	6.12	g_m/I_d Factor	118
	6.13	Technology Current	123
	6.14	Early Voltage	126
	6.15	Intrinsic Gain and Intrinsic Bandwidth	127
	6.16	Body-Effect Transconductance	130
	6.17	Summary	134
		*	
7	App	plication of Reverse Body Biasing in Analog Circuits 1	36
	7.1	Generation of On-Chip RBB Voltages	137
	7.2	RBB through Shifted Source Potential	138
		7.2.1 Analog Switch \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots	138
		7.2.2 Current Mirrors	140
		7.2.3 Common Source Amplifier Stage	142
		7.2.4 Common Drain Amplifier Stage	144
		7.2.5 Common Gate Amplifier Stage	145
		7.2.6 Two-stage Operational Amplifier	146
	7.3	Experimental Results	149
		7.3.1 Analog Switch	149
		7.3.2 Current Mirrors	150
		7.3.3 Two-stage Operational Amplifier	151
		7.3.4 Bandgap Voltage Reference	154
	7.4	SOI-MOSFET Model for Circuit Simulation	155
	7.5	Summary	156
0	G		-
8	Cor	iclusion 1	58
	8.1	Summary and Key Findings	158
	8.2	Outlook and Future Work	162
Bi	bliog	graphy 1	65
Α	Mat	terial and Measuring Methods 1	78
	A.1	Material	178
	A.2	High Temperature Oven	178
	A.3	Wafer Prober with Thermo Chuck	180
	A.4	Ceramic Chip-Package Heater	180
в	Evo	luction of Experimental Results	82
ъ	R 1	SOLMOSEET Characterization	189
	D.1		-04

Abbrevations

ABB	Adaptive body biasing
AC	Alternating current
ADC	Analog-to-digital converter
В	Body terminal
BEX	Mobility temperature exponent
BG	Back gate terminal
BJT	Bipolar junction transistor
BNC	Bayonet Neill Concelman connector
BPSG	Borophosphosilicate glass
BSIMSOI	BSIMSOI is a SPICE compact model for SOI circuit design
BT PD-SOI	Body tied partially depleted silicon on insulator
CLM	Channel length modulation
СМ	Current mirror
CMOS	Complementary metal-oxide-semiconductor
D	Drain terminal
DC	Direct current
DD	Dynamically depleted
DIBL	Drain-induced barrier lowering

EEPROM	Electronically erasable and programmable read only memory
FBB	Forward body biasing
FD	Fully depleted
FinFET	Fin field-effect-transistor
FOX	Field-oxide
G	Gate terminal
GOX	Gate oxide
GPIB	General purpose interface bus $/$ IEEE-488
HGATE	H-shaped gate SOI-MOSFET
НТ	High temperature
IC	Inversion coefficient
Isbjt	BSIMSOI model parameter for BJT injection saturation current
Isrec	BSIMSOI model parameter for recombination in depletion saturation
K1	BSIMSOI model parameter for first order body effect coefficient
LOCOS	Local oxidation of silicon
MI	Moderate inversion
MOSFET	Metal-oxide-semiconductor-field-effect-transistor
Nch	BSIMSOI model parameter for the doping concentration of the silicon film
Nfactor	BSIMSOI model parameter for the subthreshold swing factor
NHGATE	N-channel HGATE SOI-MOSFET

- NSOI N-channel Split-Source SOI-MOSFET
- op-amp Operational amplifier
- PCB Printed circuit board
- PD Partially depleted
- PHGATE P-channel HGATE SOI-MOSFET
- PID-Controller Proportional-integral-derivative controller
- PSOI P-channel Split-Source SOI-MOSFET
- PTAT Proportional to absolute temperate
- PoR Power-on reset
- RBB Reverse body biasing
- RF Radio frequency
- RFID Radio frequency identification
- RPOLY Poly-silicon resistor
- RPPLUS P^+ implanted resistor
- S Source terminal
- SCE Short-channel-effects
- SI Strong inversion
- SIMOX Separation by implantation of oxygen
- SOI Silicon on insulator
- soimod BSIMSOI model selector
- SSCB Silicon sidewall body contact
- Tbox BSIMSOI model parameter for the buried oxide thickness
- Tox BSIMSOI model parameter for the gate oxide thickness

Tsi	BSIMSOI model parameter for the silicon film thickness
UTB	Ultra thin body
VLSI	Very large scale integration
WI	Weak inversion
ZTC	Zero temperature coefficient

List of Symbols

β	Bipolar current gain
χ_{SI}	Electron affinity of silicon
$\Delta \phi$	Portion of surface potential to reach strong inversion
ΔV_{bi}	Built-in potential lowering in FD SOI-MOSFETs
ϵ_0	Dielectric constant in vacuum $8.85\cdot 10^{-9}\frac{\rm F}{\rm m}$
ϵ_{ox}	Dielectric constant of silicon-oxide $3.9 \cdot \epsilon_0$
ϵ_{si}	Dielectric constant of silicon $11.9\cdot\epsilon_0$
γ	Body effect coefficient
\hat{C}_{GBi}	Intrinsic gate-body capacitance normalized to the gate-oxide capacitance
\hat{C}_{GSi}	Intrinsic gate-source capacitance normalized to the gate-oxide capacitance
λ	Channel length modulation factor
μ_0	Zero-field mobility of charge carriers
μ_{T0}	Zero-field mobility of charge carriers at 300K
$\phi(x)$	Surface potential as a function of silicon film depth
ϕ_F	Fermi potential
ϕ_S	Surface potential
ϕ_{bi}	Built-in potential of a pn-junction
ϕ_{Fn}	Fermi potential of a n-type semiconductor
ϕ_{Fp}	Fermi potential of a p-type semiconductor
ϕ_{ms1}	Front gate metal semiconductor work function difference
ϕ_{ms2}	Back gate metal semiconductor work function difference

- ϕ_{ms} Metal semiconductor work function difference
- ϕ_{S1} Front gate surface potential
- ϕ_{S2} Back gate surface potential
- τ_q Lifetime of generated charges in the depletion region
- $\tau_n \ldots \ldots \ldots$ Lifetime of electrons
- τ_p Lifetime of holes
- A_i Intrinsic gain
- C'_D Depletion capacitance per unit area
- C'_{OX1} Front gate oxide capacitance per unit area
- C'_{OX2} Back gate oxide capacitance per unit area
- C_{DBi} Intrinsic drain-body capacitance
- C_{DSi} Intrinsic drain-source capacitance
- C_{GBi} Intrinsic gate-body capacitance
- C_{GDi} Intrinsic gate-drain capacitance
- C_{GSi} Intrinsic gate-source capacitance
- C_L Load capacitance
- C_{OX1} Front gate oxide capacitance
- C_{OX2} Back gate oxide capacitance
- C_{SBi} Intrinsic source-body capacitance
- C_{si} Capacitance of the fully depleted silicon film
- D_n Diffusion constant of electrons
- E Energy level
- E_C Conduction band energy
- $E_G(0)$ Bandgap energy at absolute zero temperature (0 K)
- $E_V \ldots \ldots$ Valence band energy
- E_F Fermi energy
- $E_G \ldots Bandgap energy$
- $E_i \ \ldots \ldots \ldots$ Intrinsic Fermi energy level

F_E	Fermi-Dirac distribution function
f_T	Intrinsic bandwidth / Transition frequency
g_m/I_d	Transconductance efficiency
g_{ds}	Drain-source small signal conductance
g_{mb}	Body-source small signal transconductance
g_{mMAX}	Maximum small signal transconductance
g_m	Small signal transconductance
I_0	Technology current
I_0 (fit)	Technology current used for fitting
<i>i_f</i>	Specific current, equivalent to I_0
I_{Bbjt}	Base current of parasitic bipolar transistor
I_B	Body current
I_{CH}	Current in the inverted channel
I_C	Collector current
I_{DIFF}	Diffusion current
<i>I</i> _{dsat}	Saturation current
I_d	Drain current
I_E	Emitter current
I_{Gmax}	Generation current at maximum depletion depth
I_G	Generation current
<i>I_{ii}</i>	Impact ionization current
I_{IN}	Input current
I_L	Leakage current
I_{OFF}	MOSFET off-state current
I_{ON}	MOSFET on-state current
<i>I</i> _{OUT}	Output current
I_{PN-N}	PN-junction leakage current of N-channel device
I_{PN-P}	PN-junction leakage current of P-channel device

xvii

I_{PN}	PN-junction leakage current
I_{PTAT}	Proportional to absolute temperature current
I_{Sub-N}	Subthreshold leakage current of N-channel device
I_{Sub-P}	Subthreshold leakage current of P-channel device
<i>ISub</i>	Subthreshold leakage current
I_S	Source current
<i>k</i>	Boltzmann constant $8.617\cdot 10^{-5}\frac{\mathrm{eV}}{\mathrm{K}}$
<i>L</i>	Channel length
L_B	Base region length
L_n	Diffusion length of electrons
<i>n</i>	Body factor
n (fit)	Body factor used for fitting
N_A	Doping concentration of p-type silicon
N_{CH}	Channel doping concentration
N_{DRAIN}	Doping concentration of drain region
N_D	Doping concentration of n-type silicon
n_{FD}	Body factor in fully depleted mode
N_I	Intrinsic region in PIN-diodes
<i>n_i</i>	Intrinsic carrier concentration
n_{n0}	Electron concentration in n-type silicon
n_{p0}	Electron concentration in p-type silicon
n_{PD}	Body factor in partially depleted mode
N_{SOURCE}	Doping concentration of source region
N_{Sub}	Effective substrate doping concentration
p_{n0}	Hole concentration in n-type silicon
p_{p0}	Hole concentration in p-type silicon
<i>q</i>	Electron charge $1.602\cdot 10^{-19}\mathrm{C}$
Q'_d	Depletion charge per unit area

Q_d	Depletion charge
Q_{ox1}	Front gate oxide charges
Q_{ox2}	Back gate oxide charges
R_B	Body resistance
<i>r</i> _{ds}	Small signal drain-source resistance
R_L	Load resistance
R_{out}	Output resistance
R_S	Source resistance
<i>S</i>	Subthreshold swing
S_{FD}	Subthreshold swing in fully depleted mode
S_{PD}	Subthreshold swing in partially depleted mode
T	Temperature
T_0	Reference temperature
T_t	Transition temperature
t_{BOX}	Back gate oxide (buried oxide) thickness
t_{OX1}	Front gate oxide thickness
t_{SI}	Silicon film thickness
TK_1	First order (linear) temperature coefficient
TK_2	Second order (quadratic) temperature coefficient
V_A	Early voltage
V_b	Body potential
V_t	Thermal voltage
V_{BGS}	Back gate-source voltage
V_{bi}	Built-in voltage of a pn-junction
V_{BN}	Body bias voltage for N-channel devices
V_{BP}	Body bias voltage for P-channel devices
V_{BSminN}	Required minimum reverse bias voltage for N-channel devices
V_{BSminP}	Required minimum reverse bias voltage for P-channel devices

V_{BSmin}	Required minimum reverse bias voltage
V_{BSN}	Body-source voltage for N-channel devices
V_{BSP}	Body-source voltage for P-channel devices
V_{BS}	External body-source voltage
<i>v</i> _{bs}	Small signal body-source voltage
V_{CM}	Common mode voltage
V_{DDA}	Supply voltage of analog circuits
V_{DSsat}	Drain-source saturation voltage
V_{DS}	Drain-source voltage
<i>v</i> _{ds}	Small signal drain-source voltage
V_{FB1}	Front gate flatband voltage
V_{FB2}	Back gate flatband voltage
V_{FB}	Flatband voltage
V_{G1}	Front gate voltage
V_{G2acc}	Back gate voltage, at which the back interface becomes accumulated
V_{G2}	Back gate voltage
V_{GNDA}	Ground potential in analog circuits
V_{GS1}	Front gate-source voltage
V_{GS}	Gate-source voltage
<i>v</i> _{gs}	Small signal gate-source voltage
V_{IN}	Input voltage
<i>v</i> _{in}	Small signal input voltage
V_{OUT}	Output voltage
<i>v</i> _{out}	Small signal output voltage
V_{REF}	Reference output voltage
V_{th1}	Front gate threshold voltage
V_{th2}	Back gate threshold voltage

- W Channel width
- W_{eff} Effective channel width
- x_{d1max} Front gate depletion depth in strong inversion
- x_{d1} Front gate depletion depth
- x_{d2} Back gate depletion depth
- phi clock signal for analog switch
- sgn Signum function

List of Tables

6.1 Doping concentrations used for TCAD simulation $\ldots \ldots \ldots$. 15
	. 101
 8.1 Comparison of NHGATE SOI-MOSFET device characteristics with applied RBB and without RBB at 400 °C. 8.2 Comparison of SOI-MOSFET device characteristics in different SOI technologies at 250 °C. 	. 159 160
	. 10

List of Figures

1.1	Operating temperature ranges according to their specific application	1
1.2	Demand for high temperature electronics divided into operating temperature ranges	2
2.1	MOSFET structure a) in bulk silicon CMOS technology and b) in SOI CMOS technology	8
2.2	Cross section of the 1.0 µm PD-SOI technology	9
2.3	Cross section of an SOI-MOSFET device, corresponding layer thicknesses and doping concentrations	10
2.4	Qualitative doping concentration of P-channel $(N_{CH} = N_D)$ and N-channel SOI-MOSFETs $(N_{CH} = N_A)$ over silicon film depth x .	11
2.5	Top view of a Split-Source N-channel SOI-MOSFET (NSOI) with source-side P^+ body contacts	11
2.6	Top view of an N-channel HGATE SOI-MOSFET (NHGATE) with a P^+ body contacts on each side of the channel	12
2.7	Photograph of an NHAGTE SOI-MOSFET in the considered SOI technology	12
2.8	Cross section of a PIN-diode in the 1.0 µm SOI technology	13
2.9	Cross section of a P^+ implanted resistor (RPPLUS) in the 1.0 µm SQI technology	14
2.10	Cross section of a poly-silicon resistor (RPOLY) in the 1.0 µm SOI technology	14
2.11	Cross section of a poly- N^+ capacitor in the 1.0 μ m SOI technology .	15
3.1	$Metal-Oxide-Semiconductor-Oxide-Semiconductor\ structure\ \ .\ .\ .$	19
3.2	Partially depleted (PD) SOI-MOSFET with a neutral body region .	19
3.3	Fully depleted (FD) SOI-MOSFET	20
3.4	x_{d1} and x_{d2} in SOI technology	23
3.5	Qualitative characteristic of the surface potentials ϕ_{S1} and ϕ_{S2} and the potential across the silicon film $\phi(x)$ in a fully depleted SOI-	
	MOSFET	26
3.6	Calculated subthreshold swing $S _{FD}$ of fully depleted SOI-MOSFETs	
	and $S _{PD}$ of partially depleted SOI-MOSFETs over temperature	29
3.7	Cross section of the PN-junction at the interface between film and source in an N-channel SOI-MOSFET with depletion width w_d and	
	built-in potential ΔV_{bi}	30
3.8	Calculated qualitative threshold voltage over temperature	34

3.9	Metal-oxide-semiconductor structure at the front gate of an SOI- MOSFET with applied film bias voltage V_B	35
3.10	Qualitative channel current of an N-channel SOI-MOSFET and	97
2 11	Illustration of the PN junction lookage current L_{-} , through the	57
0.11	reverse biased drain-film junction in a partially depleted N-channel	27
3 12	Front gate surface potential ϕ_{ce} and the Fermi potential ϕ_F	57
0.12	over temperature for $V_{GS} = 0$ V and a doping concentration of $0.8 \cdot 10^{16}$ cm ⁻³	39
3.13	Qualitative sidewall leakage current in the weak inversion input characteristic of the SOI-MOSFET	40
3.14	Top view of an NSOI-MOSFET with inversion layers on the edges of the silicon film	41
3.15	Inverted channel partially depleted SOI-MOSFET with floating body inside the silicon film region with impact ionization current	
	I_{ii} and junction leakage current I_{PN}	42
3.16	Parasitic npn bipolar junction transistor (npn-BJT) in parallel with the regular N-channel SOI-MOSFET and corresponding currents	43
3.17	Transconductance efficiency g_m/I_d over drain current I_d for different	47
9 10	Inversion coefficient in all regions of exercises i.e. from weak	47
3.10	inversion coefficient in an regions of operation, i.e. from weak inversion to strong inversion (adapted from [Bin07b])	49
3.19	Intrinsic gain stage with an N-channel SOI-MOSFET and load	50
2 20	capacitance C_L	50
3.20	Sinan signal equivalent circuit of an SOI-MOSFET for low nequencies	50
4.1	Intrinsic carrier concentration n_i and majority carrier concentration $n_0 (N_{Di})$ for different doping concentrations N_{Di} in n-type silicon	
4.0	over temperature	55
4.2	Measured threshold voltages of Split-Source NSOI-MOSFETs and NHGATE SOI-MOSFETs over temperature with $V_{BCS} = 0V$	57
4.3	Measured threshold voltage of N-channel and P-channel Split-	
	Source SOI-MOSFETs over temperature. The back gate source voltage of both devices is $V_{BGS} = 0$ V	58
4.4	Weak inversion input characteristics of an N-channel SOI-MOSFET	
	as a function of gate-source voltage V_{GS}	59
4.5	Measured normalized PN-junction leakage current of an N-channel SOI-MOSFET over temperature with $V_{GS} = -1$ V and $V_{DS} = 0.1$ V	61
4.6	Measured transconductance efficiency g_m/I_d over normalized drain current $I_d/(W/L)$ of an NHGATE SOI-MOSFET for different temperatures with $V_{DC} = 0.1$ V, $V_{DC} = 0.0$ and $V_{DCC} = 0.0$ V	62
4.7	Measured transconductance efficiency g_m/I_d of a PHGATE SOI- MOSFET for different temperatures with $V_{DS} = -0.1 \text{ V}$, $V_{BS} = 0 \text{ V}$	сл
	and $v_{BGS} = -3$ v	04

4.8	Calculated technology current I_0 of partially depleted and fully	0.7
4.0	depleted SOI-MOSFETs over temperature	67
4.5	drain current $L/(W/L)$ at 200 °C and 300 °C	68
4.10	Measured drain-source current L_d of an NHGATE SOI-MOSFET	00
1110	with channel length of 4.8 μ m and a channel width of 8 μ m at 150 °C	69
4.11	Measured Early voltage V_A as a function of normalized drain current	
	$I_d/(W/L)$ of a Split-Source NSOI-MOSFET and an NHGATE SOI-	
	MOSFET at 350 °C with a) a drain-source voltage of $V_{DS} = 2$ V and	
	b) with a drain-source voltage of $V_{DS} = 4 \text{ V}$	70
4.12	Measured Early voltage V_A as a function of normalized drain current	
	$I_d/(W/L)$ of a Split-Source NSOI-MOSFET and an NHGATE SOI- MOSEET at 400 °C with a) a drain course voltage of $V_{} = 2V$ and	
	b) with a drain-source voltage of $V_{DS} = 2$ v and	71
4.13	Intrinsic gain of NHGATE SOI-MOSFETs over drain current L_d for	
1110	a drain-source voltage of $V_{DS} = 3$ V and temperatures from 50 °C	
	up to 400 °C	72
4.14	Intrinsic gain of PHGATE SOI-MOSFETs over drain current ${\cal I}_d$ for	
	a drain-source voltage of $V_{DS} = -3$ V and temperatures from 50 °C	
	up to 400 °C	73
4.15	Calculated intrinsic bandwidth of partially depleted and fully	75
4.16	Low/Logranianter SOI-MOSPETS over temperature	10
4.10	P-channel HGATE device over temperature \dots	76
5.1	Schematic view of a symmetrical analog switch, composed of	
	HGATE SOI-MOSFET devices including charge injection compen-	Q1
52	Chip photograph of the symmetrical analog switch in the considered	01
0.2	SOI technology	82
5.3	Experimental results of the leakage current I_L over temperature at	
	the maximum of $V_{IN} - V_{OUT}$	82
5.4	Example to demonstrate the resulting error due to leakage currents	
	in analog switches	83
5.5	Basic current mirror of either a pair of a) N-channel SOI-MOSFETs	0.4
56	and b) P-channel SOI-MOSFETS	84
5.0	P-channel HCATE current mirror in the considered SQI technology	8/
5.7	a) output current I_2 over output voltage V_2 of an N-channel current	01
0.1	mirror for different temperatures. b) resulting error in percent over	
	output voltage V_2 for different temperatures $\ldots \ldots \ldots \ldots$	85
5.8	a) output current I_4 over output voltage V_4 of a P-channel current	
	mirror for different temperatures. b) resulting error in percent over	
-	output voltage V_4 for different temperatures	86
5.9	Schematic view of a two-stage operational amplifier with Miller	07
	compensation	01

5.10	Chip photograph of the two-stage operational amplifier in the considered SOI technology
5.11	Experimental results of the DC open loop gain of the two-stage operational amplifier over temperature
5.12	Schematic view of the first order bandgap voltage reference 89
5.13	Photograph of the first order handgap voltage reference in SOI
0.10	technology 90
5.14	Measurement results of the bandgap reference voltage V_{REF} over temperature
6.1	Reverse body biasing (RBB) of N-channel and P-channel SOI- MOSFETs
6.2	a) depletion depth x_{d1} over channel doping concentration and temperature without RBB ($V_{BS} = 0$ V). b) depletion depth x_{d1} over channel doping concentration and temperature with RBB ($V_{BS} = -0.4$ V)
6.3	Calculated minimum reverse bias voltage V_{BSmin} at 400 °C calculated from (6.3)
6.4	Calculated qualitative potential distribution $\phi(x)$ over silicon film depth x with a front- and back gate voltage of 0 V at a temperature of $150 {}^{\circ}{ m C}$
C F	TCAD : h c c c c c c c c
0.0	HGATE SOI-MOSFET at 50° C
6.6	Qualitative Fermi potential and front gate surface potential ϕ_{S1} over temperature
6.7	Weak inversion drain current of an N-channel SOI-MOSFET as a function of gate-source voltage V_{GS} for different temperatures from 50 °C up to 400 °C a) without RBB ($V_{BS} = 0$ V). b) with applied RBB ($V_{BS} = -1$ V)
6.8	Body factor n of an N-channel SOI-MOSFET measured as a function of temperature with a gate-source voltage of $V_{GS} = 0.7 \text{ V}$, a drain-source voltage of $V_{DS} = 3 \text{ V}$ and a back gate-source voltage of $V_{BGS} = 0 \text{ V}$ with and without applied RBB
6.9	Extracted threshold voltage V_{th} of an N-channel SOI-MOSFET over temperature and body-source voltage V_{BS}
6.10	Extracted threshold voltage over temperature and body-source voltage $V_{\rm PC}$ of a P-channel SOLMOSFET 109
6.11	Normalized PN-junction leakage current of an NHGATE SOI- MOSFET at a gate-source voltage $V_{GS} = -1$ V and a drain-source voltage of $V_{DS} = 0.1$ V without RBB (circles) and with applied
6.12	RBB (triangles)
	the back gate-source voltage is $ V_{BGS} = 0$ V

6.13	Output conductance of NHGATE and PHGATE SOI-MOSFETs with a gate-source voltage of $V_{GG} = 0.V$ at a temperature of 350 °C 114
6.14	Measurement of drain current I_d , source current I_s and body
	current I_B over gate-source voltage V_{GS}
6.15	Measurement of drain current I_d , source current I_S and body
	current I_B over temperature with and without applied RBB 116
6.16	I_{ON}/I_{OFF} ratio of N-channel SOI-MOSFETs and P-channel SOI-MOSFET over temperature with and without applied RBB 117
6.17	Measured g_m/I_d over normalized drain current $I_d/(W/L)$ of an NHGATE SOI-MOSFET for different temperature up to 400 °C with a drain-source voltage of $V_{DS} = 0.1$ V and a back gate-source voltage of $V_{BGS} = 0$ V. a) without RBB b) with applied RBB 119
6.18	Measured g_m/I_d over normalized drain current $I_d/(W/L)$ of an PHGATE SOI-MOSFET for different temperature up to 400 °C with a drain-source voltage of $V_{DS} = -0.1$ V and a back gate-source voltage of $V_{BGS} = -5$ V. a) without RBB b) with applied RBB \therefore 121
6.19	Measured g_m/I_d factor over normalized drain current $I_d/(W/L)$ of an NHGATE SOI-MOSFET at 400 °C for different drain-source voltages. a) without RBB. b) with applied RBB
6.20	Graphical extraction method of the technology current from the
	g_m/I_d curves of NHGATE SOI-MOSFETs. The drain-source
	voltage is $V_{DS} = 0.1 \text{ V}$, the back gate-source voltage is $V_{BGS} = 0 \text{ V}$
	and the body-source voltage is $V_{BS} = -1$ V
6.21	Experimentally extracted technology current I_0 of NHAGTE and PHAGTE SOI-MOSFET over temperature. The technology cur- rent was extracted up to 300 °C and extrapolated up to 400 °C [125]
6.22	Measured Early voltage of an NHGATE device with a drain-source voltage of $V_{DS} = 4$ V and a back gate-source voltage of $V_{BGS} = 0$ V a) at an operating temperature of 350 °C b) at an operating
	temperature of 400 °C
6.23	Intrinsic gain of an NHGATE SOI-MOSFET over drain current I_d at a drain-source voltage of $V_{DS} = 3$ V at temperatures from 50 °C
C 04	to 400 °C a) without RBB. b) with applied RBB
0.24	Intrinsic gain of a PHGATE SOI-MOSFET over drain current I_d at a drain-source voltage of $V_{DS} = -3$ V at temperatures from 50 °C to 400 °C a) without BBB b) with applied BBB 129
6.25	Body-Effect Transconductance a_{mb} over V_{PS} of an NHGATE device
0.20	for different temperatures
6.26	Body-Effect Transconductance g_{mb} over V_{BS} of a PHGATE device for different temperatures
7.1	a) Schematic view of a symmetrical analog switch composed of HGATE SOI-MOSFET devices including their parasitic PN-
	junction diodes. b) Qualitative leakage current over signal range $\ . \ . \ 139$
7.2	Basic current mirror with degenerated source

xxix

7.3	a) NHGATE SOI-MOSFET common source amplifier stage. b)
	Small signal equivalent circuit of a)
7.4	a) NHGATE SOI-MOSFET common drain amplifier stage. b)
	Small signal equivalent circuit of a)
7.5	a) NHGATE SOI-MOSFET common gate amplifier stage. b) Small
	signal equivalent circuit of a)
7.6	Two-stage operational amplifier using HGATE SOI-MOSFETs 147
7.7	Schematic view of a symmetrical analog switch composed of
	HGATE SOI-MOSFET devices including charge injection compen-
	sation structures
7.8	Experimental results of the overall leakage current I_L with and
	without applied RBB
7.9	Basic current mirror using RBB a) N-channel SOI-MOSFETs and
	b) P-channel SOI-MOSFETs
7.10	Output current of the NHGATE current mirror with and without
	RBB
7.11	Output current of the PHGATE current mirror with and without
	RBB
7.12	Open loop DC gain of a two-stage op-amp with and without applied
	RBB
7.13	Bandgap voltage reference using NHGATE SOI-MOSFET devices $% \mathcal{A}$. 154
7.14	Measured Bandgap reference voltage with applied RBB (V_{BN} =
	-1 V ; $V_{BP} = 6$ V) and without ($V_{BN} = 0$ V ; $V_{BP} = 5$ V) applied
	RBB
Δ 1	High temperature oven measurement setup used for DC measure-
11.1	ments of SOLMOSFET devices and circuits
A 2	a) Ceramic chin-package heater with ceramic socket and PCR h)
	Closeup of die inside chip-package and temperature gradient 181