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Approaches to Code Generation for Synchronous Transfer Architecture (STA)

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Abstract

In order to meet the ever increasing demands for higher performance, nowadays most Digital Signal Processors (DSPs) incorporate irregular architectures. However, traditional code generation and optimization techniques often fail to achieve a satisfactory code quality for irregular architectures. One important reason for this drawback is the interdependence among code generation phases involving instruction selection, register allocation and instruction scheduling. This is the well-known phase-coupling problem.

To ease this problem, three integrated code generation methods are studied based on the Synchronous Transfer Architecture (STA). The first one aims to find the optimized code by formulating the code generation as an Integer Linear Programming (ILP) problem. The second one couples instruction selection and register allocation into one phase with a two-step register allocator. The third one combines register allocation and instruction scheduling by using greedy algorithms that are widely used for network planning and optimization. All these methods have been implemented in a Matlab compiler for a SIMD-VLIW STA-based processor. In this thesis, it will be shown that much better performance can be achieved by the integrated code generation in comparison to that obtained in the conventional way.

Besides the studies on the SIMD processor, the commercial Compiler development System (CoSy) is applied to generate assembly code for a scalar, VLIW, STA-based processor. Because of the architectural features of this processor, some adaptations for STA data transfer and addressing mode have been carried out in the code generation.

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