

Lehrstuhl für Netzwerktheorie und Signalverarbeitung  
Technische Universität München

# **Contributions to the Methodology of VLSI Circuit Design**

Marek Wróblewski

Vollständiger Abdruck der von der Fakultät für Elektrotechnik und Informationstechnik der Technischen Universität München zur Erlangung des akademischen Grades eines

Doktor-Ingenieurs  
genehmigten Dissertation.

Vorsitzender: *Univ.-Prof. Dr.-Ing. Ulf Schlichtmann*  
Prüfer der Dissertation:

1. *Univ.-Prof. Dr. techn. Josef A. Nossek*
2. *Univ.-Prof. Dr.-Ing. Klaus Diepold*

Die Dissertation wurde am 04.10.2004 bei der Technischen Universität München eingereicht und durch die Fakultät für Elektrotechnik und Informationstechnik am 28.01.2005 angenommen.



Berichte aus dem Lehrstuhl für Netzwerktheorie und  
Signalverarbeitung der Technischen Universität München

**Marek Wróblewski**

**Contributions to the Methodology  
of VLSI Circuit Design**

Shaker Verlag  
Aachen 2005

**Bibliographic information published by Die Deutsche Bibliothek**

Die Deutsche Bibliothek lists this publication in the Deutsche Nationalbibliografie; detailed bibliographic data is available in the internet at <http://dnb.ddb.de>.

Zugl.: München, Techn. Univ., Diss., 2005

Copyright Shaker Verlag 2005

All rights reserved. No part of this publication may be reproduced, stored in a retrieval system, or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording or otherwise, without the prior permission of the publishers.

Printed in Germany.

ISBN 3-8322-3884-0

ISSN 1433-1446

Shaker Verlag GmbH • P.O. BOX 101818 • D-52018 Aachen

Phone: 0049/2407/9596-0 • Telefax: 0049/2407/9596-9

Internet: [www.shaker.de](http://www.shaker.de) • eMail: [info@shaker.de](mailto:info@shaker.de)

## Acknowledgements

This work is the result of my research activities at the Institute for Network Theory and Signal Processing at the Technische Universität München. It would not have been possible without the continuous support from Prof. Dr. tech. Josef A. Nossek, whom I would like to thank for giving me the opportunity to freely investigate numerous paths along the way. Furthermore, I would like to thank Prof. Dr.-Ing. habil. Walter Entenmann for leading the VLSI group, as well as Prof. Dr.-Ing. Klaus Diepold for reviewing this thesis.

For the pleasant atmosphere during my work at the institute I thank all the people who make up the NWS, especially Mrs. Zelt, Mrs. Heer and Mrs. Barth for their support in various administrative issues, as well as the research assistants who, with time, have become more than just companions.

With great pleasure I look back at the time spent together with the other members of the VLSI group: Andreas Schlaffer, Christian Schimpfle, Christoph Saas, Dirk Waldhauser and Matthias Müller who contributed more than just one idea to this work. I owe more than a simple "thank you" to Prof. Dr.-Ing. Sven Simon who showed me how to never give up.

Oliver Riesener, who first introduced me to the sunny side of life, and Sergei Fedorov, both deserve my gratitude for those countless evenings in the air conditioned room.

Finally, there are my parents and my brother Artur, who stood by me and helped, each in their own way, where no help could be hoped for.

München, in March 2005



# Inhaltsverzeichnis

<b>1. Introduction</b>	<b>1</b>
1.1 Sample rate conversion . . . . .	2
1.2 Low power aspects of VLSI design . . . . .	3
1.2.1 Sources of power dissipation in CMOS circuits . . . . .	3
1.2.1.1 Capacitive component $P_{cap}$ . . . . .	3
1.2.1.2 Short circuit component $P_{sc}$ . . . . .	5
1.2.1.3 Leakage component $P_{leak}$ . . . . .	5
1.2.1.4 Dominant components . . . . .	6
1.2.2 Glitching . . . . .	6
1.2.3 Methods of power reduction . . . . .	7
1.3 Programmable architectures . . . . .	8
<b>2. Configurable sample rate conversion based on the Farrow structure</b>	<b>11</b>
2.1 Introduction . . . . .	11
2.1.1 Problem formulation . . . . .	11
2.2 The Farrow structure . . . . .	11
2.3 Implementation issues of the Farrow structure . . . . .	14
2.4 Extension of the Farrow structure . . . . .	16
2.4.1 Computation of the intersample position . . . . .	16
2.4.2 Scope of investigations . . . . .	17
2.4.3 Boundary of clock domains . . . . .	18
2.4.4 Ring buffer structure . . . . .	18
2.4.4.1 Ring buffer . . . . .	18
2.4.4.2 Input ring buffer control block . . . . .	20
2.4.4.3 Output ring buffer control block . . . . .	20
2.5 Control structures . . . . .	21
2.5.1 Estimation of the ratio of clock periods . . . . .	21
2.5.2 Elimination of quantization impact . . . . .	23
2.5.2.1 Error condition detection . . . . .	25
2.5.2.2 Ideal situation . . . . .	26
2.5.2.3 Adaptive loop . . . . .	26
2.5.2.4 Reduction of settling time . . . . .	30
2.5.2.5 Detection of $p$ . . . . .	32
2.5.2.6 Remarks on metastability . . . . .	32

2.5.3	Phase detection . . . . .	33
2.6	Interpolation quality and quantization effects . . . . .	33
2.6.1	Conclusions . . . . .	43
<b>3.</b>	<b>Reduction of spurious switching activity of cyclic circuits</b>	<b>45</b>
3.1	Introduction . . . . .	45
3.2	Motivation . . . . .	47
3.2.1	Retiming . . . . .	47
3.2.2	Slowdown . . . . .	50
3.2.3	Clock phases . . . . .	53
3.2.3.1	General considerations . . . . .	53
3.2.3.2	Generation of clock signals . . . . .	54
3.2.3.3	Assignment of clock phases . . . . .	56
3.3	Principle . . . . .	58
3.4	Algorithm . . . . .	60
3.4.1	Selection of factor $m$ . . . . .	60
3.4.2	Slowdown . . . . .	61
3.4.3	Cost function . . . . .	61
3.4.4	Retiming . . . . .	61
3.4.5	Clock phases . . . . .	66
3.4.6	Removal of superfluous registers . . . . .	70
3.5	Simulation results . . . . .	70
3.5.1	Circuit 1: A lattice IIR filter . . . . .	71
3.5.2	Circuit 2: A cascaded IIR filter . . . . .	75
3.5.3	Circuit 3: A structure for polynomial evaluation . . . . .	75
3.5.4	Circuit 4: A MAC unit . . . . .	78
3.6	Conclusions and outlook . . . . .	80
3.6.1	Automated low-power retiming . . . . .	80
3.6.2	Resolution of timing constraints . . . . .	83
3.6.3	Summary . . . . .	84
<b>4.</b>	<b>Low-power design method for synthesizable register files</b>	<b>85</b>
4.1	Motivation . . . . .	85
4.2	Method . . . . .	88
4.3	Limitations . . . . .	89
4.4	Timing . . . . .	90
4.4.1	Clock gating related timing issues . . . . .	90
4.4.2	Timing issues related to physical placement . . . . .	92
4.5	Simulation results . . . . .	93
4.6	Conclusions . . . . .	95
<b>5.</b>	<b>Summary</b>	<b>97</b>
<b>Appendix</b>		<b>99</b>
<b>Bibliography</b>		<b>103</b>