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# Contributions to the Methodology of VLSI Circuit Design

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# Contributions to the Methodology of VLSI Circuit Design

This work presents a concept of implementing a sample rate conversion VLSI circuit based on the Farrow structure. It focuses mainly on reliable data transfer from one clock domain to the other. Towards this end an architecture based on a ring buffer is given, whose control structure compensates the inevitable quantization errors. This enables highest interpolation quality, which is only insignificantly inferior to the theoretically achievable results.

Furthermore, two low-power design methods for digital CMOS circuits are presented. The reduction of both the switching activity as well as the switched capacitance is targeted. An algorithmic procedure is devised, as well as concepts for alleviating the influence of the applied steps on timing. The effectiveness of the methods is demonstrated by means of simulations of test circuits.