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A Property Checking Methodology for Weakly Programmable System-on-Chip IPs

Eine Methode zur Eigenschaftsprüfung von schwach programmierbaren System-on-Chip IPs

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Over the last years we have seen an increasing trend towards application specific instruction set processors that are designed in order to meet the required flexibility, energy efficiency and performance constraints. In its extreme extend these processors are that specialized that they only offer a limited programmability meeting exactly the demands of the targeted application domain. Such processors are called weakly programmable system-on-chip IPs (WPIP). The focus of these WPIPs is to offer just as much flexibility as required while delivering energy efficiency and performance comparable to that of custom hardware. A main characteristic of these WPIPs is a customized memory architecture with memories being accessed from several pipeline stages.

It turns out that the design flow followed by the designers of such WPIP designs hampers the validation of these IPs. On the one hand simulation based approaches can not achieve a sufficient coverage. Formal verification techniques, on the other hand, can achieve a sufficient coverage, however, the design flow and distributed memory architecture forbid the usage of the verification techniques as they are used in today's formal verification of standard processors.

This dissertation presents a systematic approach to completely verify these WPIP designs. A main aspect of the presented technique is that the verification engineer is only required to specify the intended behavior at the level of well documented pipeline operations resulting in the operational ISA (OISA) model introduced in this work. The additional information required to handle the side-effects of the distributed memory access as well the behavior ensuring that the property set is complete are automatically generated by an analysis of the OISA model.

For WPIPs software and hardware are tightly coupled together making it important to ensure that the combined hardware software system is working correctly. The second part of this work presents how to reuse the property set from the hardware verification for the verification of the software.

The presented approach is demonstrated at the example of two WPIPs for channel decoding. Even so these WPIPs were intensively simulated beforehand several bugs were discovered with the presented formal verification methodology.