
Path Predicate Abstraction

for Sound System-Level Modeling of Digital Circuits

Vom Fachbereich Elektrotechnik und Informationstechnik
der Technische Universität Kaiserslautern
zur Verleihung des akademischen Grades

Doktor der Ingenieurwissenschaften (Dr.-Ing.)

genehmigte Dissertation von

Joakim Henrik Urdahl
geboren in Lærdal, Norwegen

D 386

Datum der mündlichen Prüfung:	15. Dezember 2015
Dekan des Fachbereichs:	Prof. Dr.-Ing. Hans D. Schotten
Vorsitzender der Prüfungskommission:	Prof. Dr. Gerhard Fohler
Gutachter:	Prof. Dr.-Ing. Dr. Wolfgang Kunz Prof. Dr.-Ing. Kjetil Svarstad, NTNU

Berichte aus der Elektronik

Joakim Urdahl

Path Predicate Abstraction

for Sound System-Level Modeling of Digital Circuits

D 386 (Diss. Technische Universität Kaiserslautern)

Shaker Verlag
Aachen 2016

Bibliographic information published by the Deutsche Nationalbibliothek

The Deutsche Nationalbibliothek lists this publication in the Deutsche Nationalbibliografie; detailed bibliographic data are available in the Internet at <http://dnb.d-nb.de>.

Zugl.: Kaiserslautern, TU, Diss., 2015

Copyright Shaker Verlag 2016

All rights reserved. No part of this publication may be reproduced, stored in a retrieval system, or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording or otherwise, without the prior permission of the publishers.

Printed in Germany.

ISBN 978-3-8440-4233-7

ISSN 1436-3801

Shaker Verlag GmbH • P.O. BOX 101818 • D-52018 Aachen

Phone: 0049/2407/9596-0 • Telefax: 0049/2407/9596-9

Internet: www.shaker.de • e-mail: info@shaker.de

Acknowledgments

This thesis documents several years of research carried out while I have been part of the “electronic design automation group” at the University of Kaiserslautern. During this entire period the work has been conducted in the close collaboration of our group.

Specifically, I would like to mention Markus Wedler, Binghao Bao and Shrinidhi Udipi for their contributions to research employed in this thesis, Christian Bartsch for his help with the German summary, and Carmen Vicente-Fess for organizing my life.

Most of all, I would like to especially thank my supervisors, Prof. Wolfgang Kunz and Prof. Dominik Stoffel, who have been as dedicated to this research as myself during all these years. Thank you for all your time and your incredible devotion to our research. I am extremely proud that you have let me work with you.

Many thanks also to Prof. Kjetil Svarstad for his in-depth analysis in the review of this thesis and to Prof. Gerhard Fohler for chairing the examination procedures.

To all friends that have made my time in Germany cheerful.

To my family, thank you for supporting me. I look forward to see more of you.

Kaiserslautern, 14.01 2016
Joakim Urdahl

Contents

Acknowledgments	iii
1 Introduction	1
1.1 Abstract Circuit Descriptions	2
1.1.1 Transistor Level	2
1.1.2 Gate Level	2
1.1.3 Register Transfer Level	3
1.1.4 Electronic System Level	4
1.1.5 The Semantic Gap	5
1.2 Verification in Industrial Practice	7
1.2.1 Simulation	8
1.2.2 Coverage	9
1.2.3 Assertions	10
1.3 Motivation and Overview	11
1.4 Publication List	13
2 Reasoning in Circuits	15
2.1 Modeling Sequential Behavior	15
2.1.1 Finite State Machine	15
2.1.2 Kripke Model	16
2.1.3 Labeled Transition System	17
2.2 Temporal Logic	17
2.2.1 Computation Tree Logic	18
2.2.2 Linear Temporal Logic	19
2.2.3 CTL*	19
2.3 Automated Theorem Proving	20
2.4 Model Checking	20
2.4.1 CTL Model Checking	20
2.4.2 LTL Model Checking	21
2.4.3 Bounded Model Checking	22
2.4.4 Interval Property Checking	23
2.4.5 k -step Induction	25
2.5 Abstraction Techniques	25
2.5.1 Bisimulation	25
2.5.2 Stuttering Bisimulation	26
2.5.3 Bisimulation modulo Silent Actions	27

2.5.4	Localization Reduction	28
2.5.5	Predicate Abstraction	28
3	Complete Interval Property Checking	29
3.1	Terminology	29
3.2	Completeness Criterion	32
3.3	Completeness Check	32
3.3.1	Case Split Test	34
3.3.2	Successor Test	34
3.3.3	Determination Test	35
3.3.4	Reset Test	36
4	Path Predicate Abstraction	37
4.1	Path Predicate Abstraction for Directed Graphs	38
4.2	Path Predicate Abstraction for FSMs	40
4.3	Operational Coloring by C-IPC	46
4.4	Model Checking with Path Predicate Abstraction	50
4.5	Comparison with other Abstraction Techniques	54
5	Compositional Path Predicate Abstraction	57
5.1	Abstract System Model	57
5.2	Communication schemes in digital hardware	60
5.3	Modeling Communication	60
5.4	Synchronization and wait-stuttering	64
5.5	Model checking on abstract system	67
6	Practical Methodology	71
6.1	Abstraction Flow	71
6.2	Example Design	72
6.3	Obtaining a complete property set	74
6.4	Creating a compositional abstraction	78
6.5	Experimental Results	80
6.5.1	Case Study:Flexible Peripheral Interconnect (FPI) bus	80
6.5.2	Case Study: SONET/SDH Framer	81
7	A Novel Design Flow	83
7.1	Design Flow	83
7.2	Architectural Modeling Language	86
7.2.1	Global Scope	86
7.2.2	Example	87
7.2.3	Module Definitions	88
7.3	Correct Refinement	89
7.3.1	Objects of the Abstraction	90
7.3.2	Operational Structure	91
7.3.3	Modeling Communication at the RTL	91
7.4	Experimental Results	92
7.4.1	Student Project	92

8 Perspectives for Low-Power Design	95
8.1 Energy Estimation at System Level	95
8.1.1 Energy Estimation for GCD circuit	96
8.2 Dependency Analysis for Power Optimization	100
8.3 Power Aware Design Flow	101
9 Conclusion	103
Bibliography	105
Kurzfassung in Deutsch	111
Pfadprädikatenabstraktion (PPA)	112
Anwendungsverfahren	113
Perspektiven für Energiesparende Entwürfe	114
Appendix A AML Syntax	117
Appendix B Design Flow Demonstrator: Monitor	121
B.1 Architectural Description	121
B.2 Operation Property Suite	122
Appendix C Design Flow Student Project	131
C.1 Architectural Description	131
C.2 Operation Property Suite	131
C.3 RTL implementation	131